A New Class of Single Event Hard Errors

Recoverable and Nonrecoverable Hard-Errors in DRAMs†

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Introduction

Hard errors from single-ion interactions in static CMOS memories were first reported in 1991 ,[1] and have been the subject of several additional investigations.[2,3] Oldham has developed a model for hard errors which is consistent with the localized dose deposited by an ion that strikes the gate region. [3] His model gives reasonable agreement with the statistics of hard errors, assuming that two or more ions must strike the sensitive region during the course of an experiment. He also noted that this type of hard error was only observed in 4-T cell structures, which have extremely large polysilicon load resistors, and suggested that the mechanism would be less important for future scaled designs, because of the trend toward active thin-film load transistors in future designs.

This paper reports on hard errors induced by single ions in dynamic memories. For ions with atomic number below 80, hard errors in DRAMs appear to be similar to the hard errors reported in previous work on SRAMS. Onc feature of these hard errors is that they tend to recover gradually with time, because of annealing, and arc thus partially recoverable. However, for gold ions, a second type of hard error was discovered which is not recoverable, and appears to be due to catastrophic internal shorting rather than small changes in leakage current. '1'bus, nonrecoveable errors will likely occur even in devices which eliminate the extreme sensitivity to leakage current that is inherent in 4-T SRAMS and DRAMs. It is important to understand the mechanism that is responsible for nonrecoverable errors, and investigate the effect of device scaling.

Experimental Procedure

Several different memories were selected for this study, but data in the summary will concentrate on one device, a 4 Mbit DRAM from OKI Semiconductor. These devices were fabricated in 1992, and had a feature size of 0.8 μm with an oxide thickness of 15 nm. Internal operating voltage is 5 V. The manufacturer has since modified the process; current devices have a feature size of 0.6 pm with an oxide thickness of 12 nm. Test results for the new process will be provided in the complete paper.

A number of tests were done at the Brookhaven National Laboratory using heavy ions wit h ranges of 40 μm or more. The ion with the highest atomic number was gold. Tests were done at normal incidence, as well as with angles up to 60 degrees. Because hard errors arc permanent, separate test devices were required for each ion species and angle.

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Hard errors were determined in two ways. One obvious way is simply to measure the number of failed bits, using the minimum refresh time specified by the manufacturer. However, it is also possible to directly measure the data retention time, which allows quantitative evaluation of leakage currents of all storage cells within the memory. 'l'his is a powerful diagnostic technique for hard errors in DRAMs because it provides a statistical distribution of total dose damage in the entire memory array, and is thus a good indicator of the amount of localized damage induced by ions in individual cells.

Recoverable and Nonrecoverable Error Results

A summary of experimental results for the OKI 4 Mbit DRAM is shown in Figure 1. This figure shows the distribution of data retention time for three devices that were exposed under different conditions: (1) gold at normal incidence (1 .ET = 82 MeV-mg/cm^2); (2) gold ata600 angle (I .ET = 164 MeV-mg/cm^2); and (3) iodine at a600 angle (1.1'3' = 120 MeV-mg/cm^2). When the device was irradiated with iodine at high angle, there is a smooth distribution of refresh times, consistent with ions striking various regions at and near the gate. However, much different results were obtained for the two irradiations with gold ions. A significant number of errors occur with extremely short refresh times (these bits have actually failed catastrophically). This distribution is superimposed on a gradual distribution of refresh times that is similar to the iodine results. The distribution in the Figure corresponds to approximately 2 x 10^4 bits in the memory array.

Note that even though the LET of the iodine ions is well above the LET of gold at normal incidence, no nonrecoverable errors were ever observed with iodine. Furthermore, approximately the same number of nonrecoverable errors occurred for gold at normal and high angle incidence, which have very different effective LET. These results show that the nonrecoverable errors do not appear to scale with angle, which is generally assumed for most single-particle testing (single-c.vent burnout is an important exception). This has importance consequences for radiation testing as well as for calculation of the expected number of nonrecoverable errors in a real space environment.

The nonrecoverable errors arc also not additive; i.e., damage from several interactions at or near the gate does not appear to cause this type of error, because no nonrecoverable errors were ever observed for ions with Z below gold, even when they were exposed to relatively large ion fluences.

Retention time tests were done on devices at long time periods - up to several months - after the heavy-ion testing was completed. Over long time periods, the percentage of "weak" bits, i.e., hard errors induced by ions with lower atomic number that have a smooth distribution of data retention time, gradually decreased. l'bus, these hard errors are partially recoverable, even at room temperature. On the other hand, *no* recovery was observed for any of the hard errors with catastrophic failure that were induced by gold.

Additional evaluation of the two types of hard errors was done in the laboratory, using an Advantest test system that allowed more complete measurements to be made. These tests showed that the "weak" bits were caused by increased leakage between the $V_{dd}/2$ reference line, internal to the memory, and the individual pass transistors. This is

essentially the same mechanism reported by Oldham for SRAMS, although the details are different in the DRAM implementation. 'l'he nonrecoverable errors appear to be caused by an internal short circuit between the pass transistor and V_{dd}. l'bus, the internal mechanisms associated with the two types of hard errors at-e clearly different. Further details will be provided in the complete paper.

Effects of Gamma Irradiation on Data Retention Time

In order to relate the data retention time observed from accelerator testing to conventional total dose damage, some devices were tested in a cobalt-60 source, measuring the retention time distribution after a series of successive irradiations. These results are shown in Figure 2. Note that unlike the heavy ion results, a very steep distribution is observed for retention time after total dose irradiation. This is expected, because damage from individual gamma interactions is far below the damage threshold for these devices. From this figure, it is apparent that the. retention time technique can detect total dose effects in indvidual bits at levels of only a few thousand rad(Si). Furthermore, it changes gradually with increasing levels of total dose, as expected with the assumption that the retention time increase is due to subthreshold leakage changes in the pass transistors.

Discussion

Clearly the existence of nonrecoverable errors is extremely important in system applications. The preceding discussion shows that nonrecoverable bard errors behave quite differently than the recoverable hard errors reported in SRAMs, and suggests that the mechanism that is responsible is quite different from the microdose mechanism that appears to bc the cause of recoverable errors. Some characteristics of nonrecoverable errors such as the apparent failure of the cosine law arc similar to characteristics exhibited by gate rupture in power devices.[4]

Additional tests are planned on these devices that should provide further insight into the mechanism, along with effects of scaling. These include tests of the scaled OK] device, which has a thinner gate oxide, tests at elevated temperature, and tests with different internal gate voltage (i.e., forci ng the internal $V_{dd}/2$ linc to a different value), as well as data on additional part types from different manufacturers.

The question of scaling is vital for this mechanism, because the reduction in power supply voltage that is planned for future devices will result in reduced oxide thickness. If nonrecoverable error rates increase with this t ypc of sealing, then this mechanism may bc a dominant factor in applying future VI S] devices in space systems.

References

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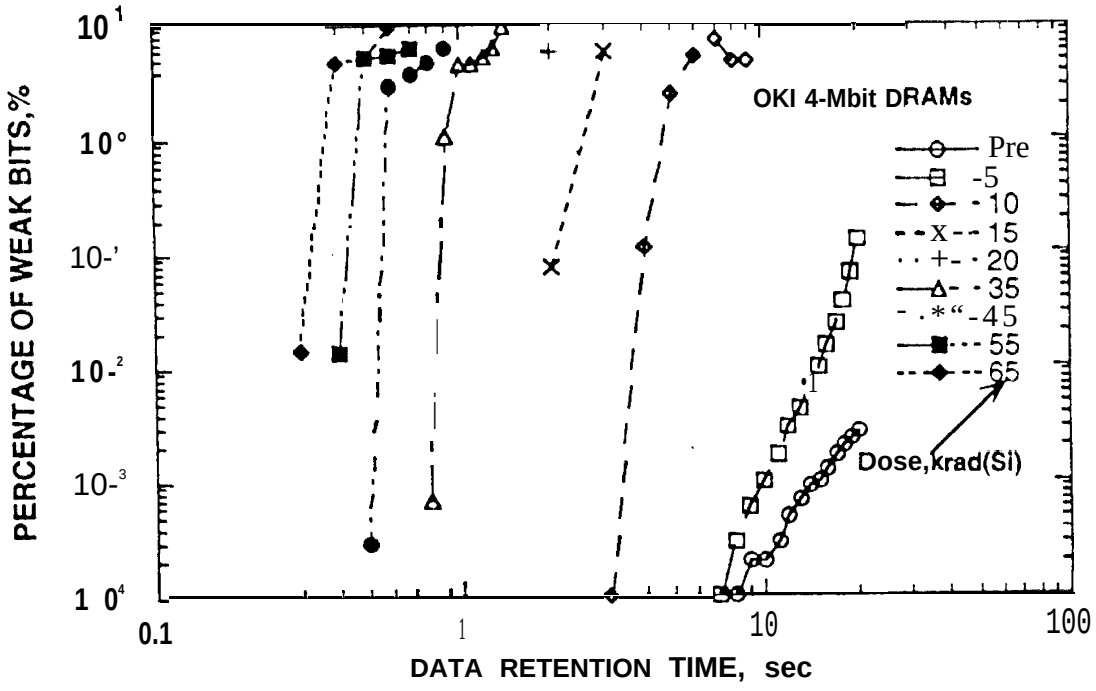

Figure 1. Percentage of DRAM bits with data retention time less than the value on the abscissa. A single mechanism dominates the iodine data, while two mechanisms are responsible for the behavior of DRAMs that were irradiated with gold.

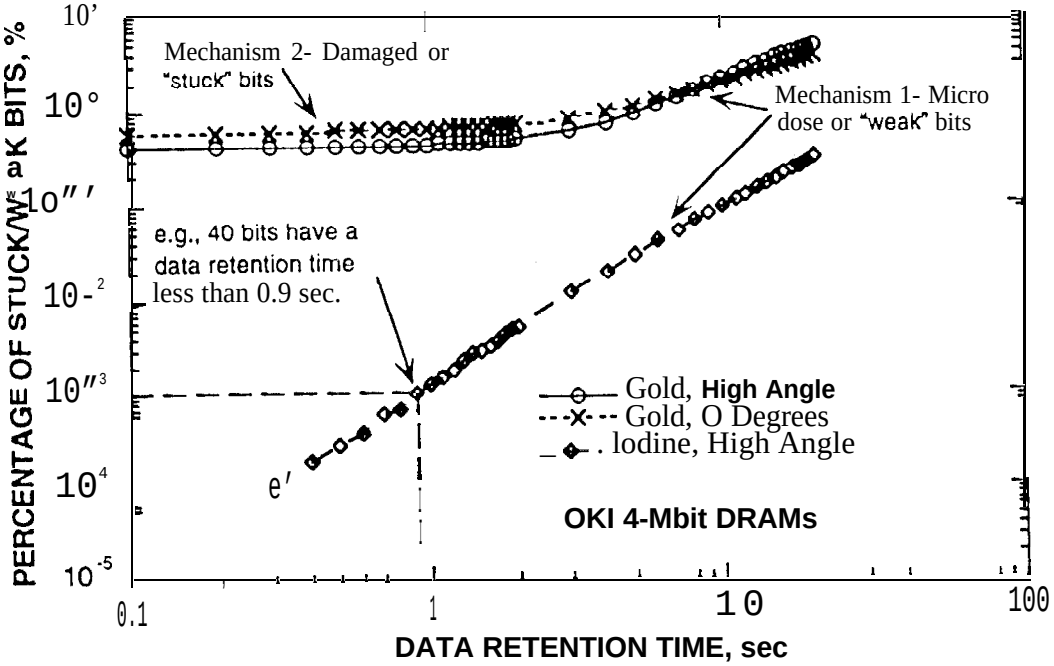

Figure 2. Change in retention time for DRAMs irradiated with cobalt-60 gamma rays. Note the sharp threshold, corresponding to nearly uniform damage in all bit locations, compared to the data for iondinc in Figure 1.